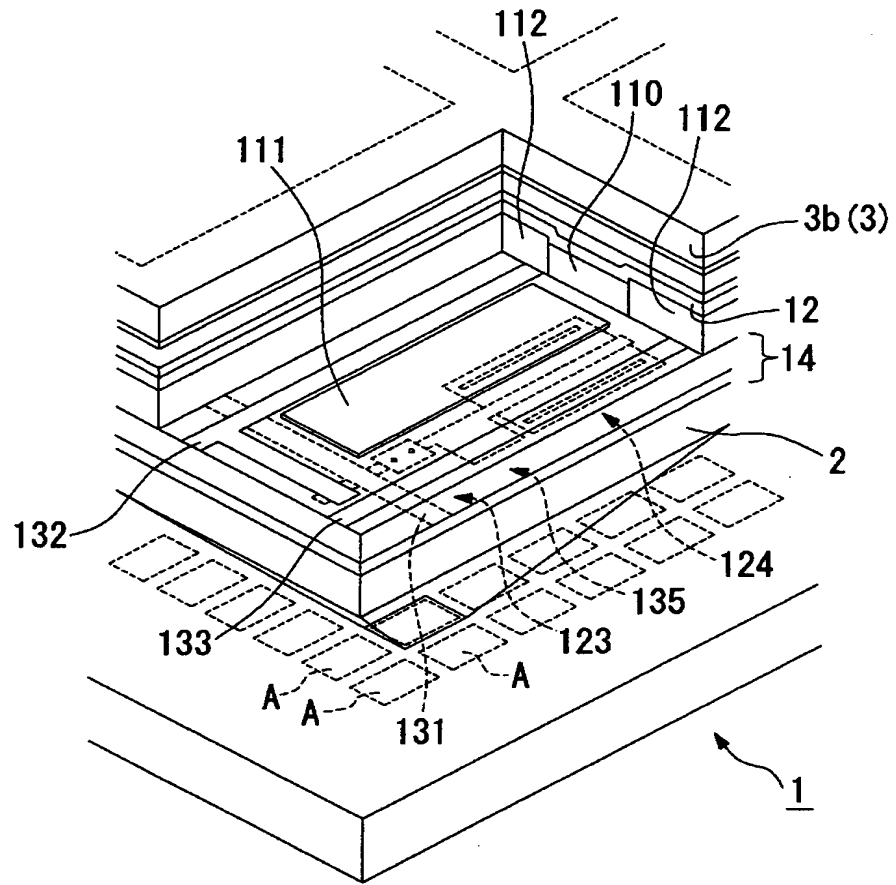


FIG. 1



This cross-sectional diagram illustrates a multi-layered semiconductor device. The top surface features three distinct regions labeled R, G, and B, each containing a series of rectangular patterns (110b, 110a, 110b₁, 110b₂, 110b₃) separated by spacers (111). These patterns are situated on a common base layer (110). Below this, a thick substrate (123) contains several horizontal layers: a conductive layer (141), an insulating layer (142), another conductive layer (143), and a final insulating layer (144). Vertical vias or pillars (145, 146) connect the upper patterns to the lower conductive layers. A central vertical channel (147) is also present. The entire assembly is capped by a thin layer (10) and a protective coating (2c).

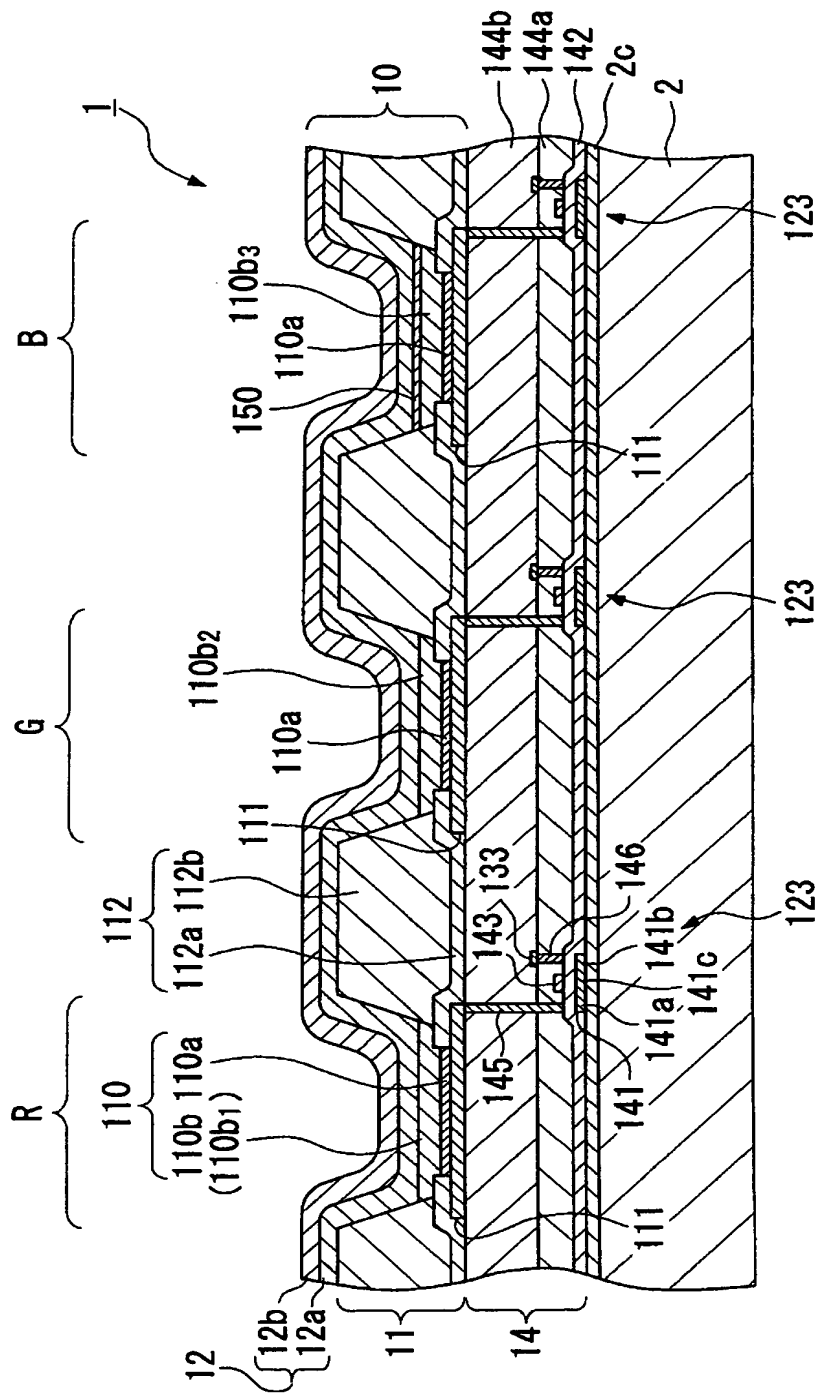


FIG.4A

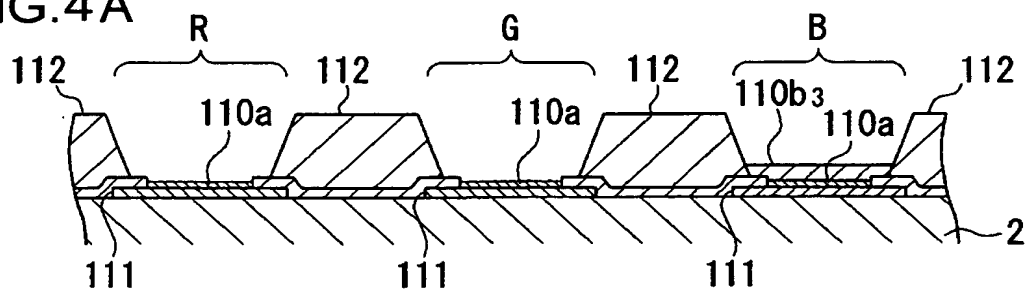


FIG.4B

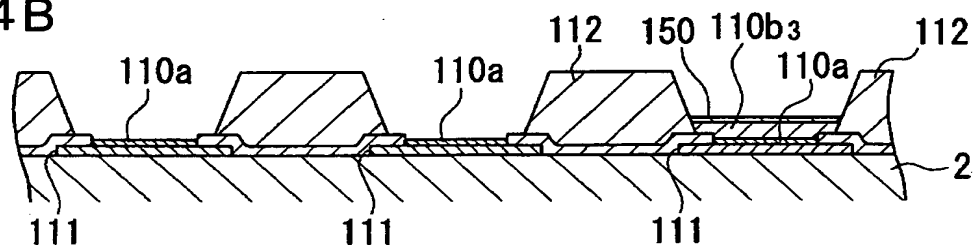


FIG.4C

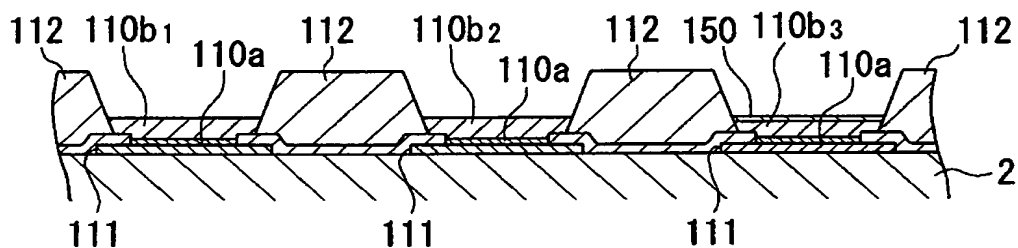


FIG.4D

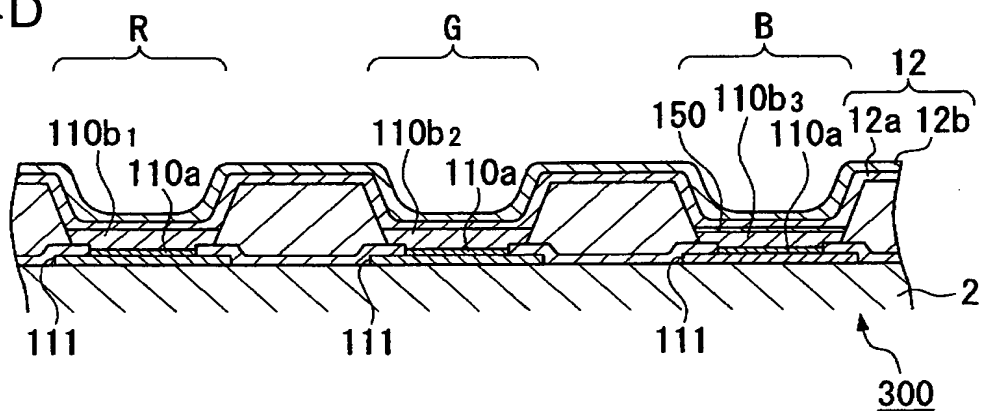


FIG.5A

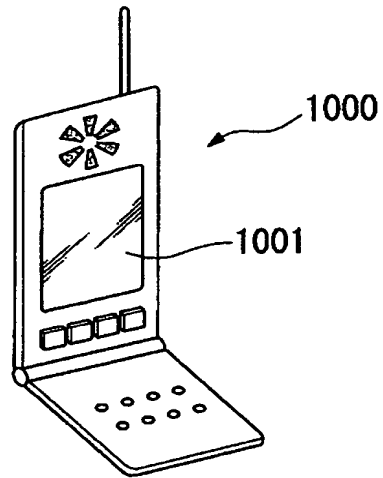


FIG.5B

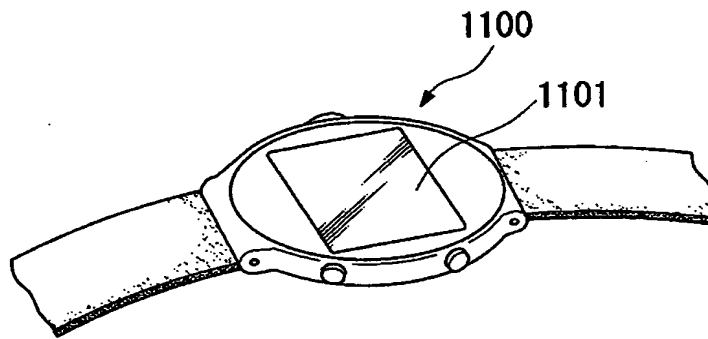


FIG.5C

